Amendments to the Specification:

Page 5, lines 14-15, amend the paragraph as follows:

Figure 4A is diagrammatic representation of a DES engine 213 as shown in Figure 2.

Figure [[4]] 4B is a diagrammatic representation of a DES engine in accordance with one embodiment of the present invention.

Page 13, lines 16-30, amend the paragraph as follows:

As will be appreciated by one of skill in the art, various control signals may be used. An alternative approach would be to use a 3-to-1 single level multiplexer to select either the initial data, the swapped feedback data, or the non-swapped feedback data. The use of a 3-to-1 single level multiplexer however adds significant delay to the timing critical datapath because the 3-to-1 multiplexer can not be easily combined with the registers. The 3-to-1 multiplexer uses an extra clock cycle. According to a preferred embodiment, four 2-to-1 multiplexers are used. The 2-to-1 multiplexers in the second level of the multiplexer stage 409 can be integrated with the registers 411 and 413. Register 411 contains the last half of this initial 64-bit block in round 1. Register 413 contains the right half of the 64-bit block in round 1. Registers 411 and 413 both typically hold 32-bits of data. The 32-bit data block contained in register 413 is provided to both expansion stage 415 and to register 411 through multiplexer stage 409 for the next round. Control signals in multiplexer stage 409 are

configured to provide the 32-bit data block contained in register 413 to register 411 in the next round of DES processing. The 32-bit data block is provided to expansion logic 415.

Page 21, lines 22-26, amend the paragraph as follows:

In the third stage, also called the ~~prorogation~~ propagation stage, the round is passed from the key scheduler to the round logic. The round key is registered at register 623 in Figure 6 or is input at inp1 705, inp2 707, and inp3 at 709. In the fourth stage also called the consumption stage, the round key is used in the corresponding DES round. As shown in table 1 below, the key scheduler takes advantage of pipeline processing.